Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VS+**
2. **OE**
3. **IN**
4. **GND**
5. **VS-**
6. **VL**
7. **OUT**
8. **VH**

**.060”**

**.061”**

**EL7155**

**MASK**

**REF**

**1**

**2**

**3**

**4 5**

**8**

**7**

**6**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: EL7155**

**APPROVED BY: DK DIE SIZE .060” X .061” DATE: 4/25/22**

**MFG: INTERSIL THICKNESS .013” P/N: EL7156**

**DG 10.1.2**

#### Rev B, 7/1